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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,342	12/11/2003	Sweyyan Shei	FORT 2769	3750

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SMITH-HILL AND BEDELL, P.C.
16100 NW CORNELL ROAD, SUITE 220
BEAVERTON, OR 97006

EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,342	SHEI ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-24 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 6/16/03 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-3, 5-10, 12, 13, 17, 19, 20, 22, and 23** are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Sample et al. (US Patent Application Pub. No. 2003/0074178)**, herein referred to as Sample.

As per **claim 1**, Sample is directed to an apparatus for performing an emulation of an electronic circuit and for transmitting and receiving, via a network, packets conveying data relating to the emulation, the apparatus comprising:

a. a circuit board [0100]

b. at least one emulation resource mounted on the circuit board, each for emulating a behavior of at least a portion of the electronic circuit by producing output signals in response to input signals in a manner controlled by input programming data [0015], [0100]. The logic board consists of a plurality of field-programmable gate arrays, which are used to emulate portions of a circuit.

c. a network/resource interface circuit mounted on the circuit board for transmitting input signals to the at least one emulation resource, the input signals being of states controlled by data conveyed by packets arriving via the network, and for transmitting on the network packets conveying data representing states of output signals produced by the at least one emulation resource [0108], [0122]. The logic board contains a VME interface (i.e. an interface to the CPU). The CPU provides a network interface and overall control of the emulation system.

As per **claim 2**, Sample is directed to the apparatus in accordance with claim 1 further comprising: random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data representing states of *output signals* produced by the at least one emulation resource in the RAM during the emulation and thereafter transmits on the network packets conveying the data it stored in the RAM [0015], [0189], [0191].

As per **claim 3**, Sample is directed to the apparatus in accordance with claim 1 further comprising: random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data conveyed by packets arriving via the network in the RAM prior to performing the emulation, and then controls states of inputs signals it transmits to the at least one emulation resource in response to the data it stored in the RAM [0111].

As per **claim 5**, Sample is directed to the apparatus in accordance with claim 1 wherein the at least one emulation resource comprises a plurality of programmable logic devices (PLDs) each having a plurality of terminals for receiving its input signals and for transmitting its output signals [0066], and wherein the apparatus further comprises: a first plurality of signal paths formed on the circuit board linking a first subset of the terminals of each PLD to terminals of others of the PLDs for conveying their output signals to one another [0066]. The PLD's are interconnected using the partial crossbar interconnect [0066] and each physical interconnection represents one or more design signals. These physical interconnections are analogous to the signal paths in the claim language.

As per **claim 6**, Sample is directed to the apparatus in accordance with claim 5 wherein each PLD comprises a field programmable gate array (FPGA) [0066].

As per **claim 7**, Sample is directed to the apparatus in accordance with claim 5 further comprising: a bus, formed on the circuit board and connected in parallel to a second subset of the

terminals of each PLD, for conveying input and output signals between each PLD (figure 11 bus 4; figure 12 bus 202) and the network/resource interface circuit (figure 11 bus 310). The logic chip contains a VME interface (figure 20 interface 222) that is connected to the CPU (figure 20 processor 700) that provides the network interface. Thus 32 bit VME bus (figure 20 bus 600) allows exchange of data between the logic board and the CPU.

As per **claim 8**, Sample is directed to the apparatus in accordance with claim 5 wherein

a. the network/resource interface circuit generates at least one clock signal [0104], and wherein the apparatus further comprises:
b. a clock bus connected between the network/resource interface circuit and each PLD, for concurrently delivering edges of the at least one clock signal to each PLD for clocking logic circuits within the PLDs during the emulation [0104-0105].

As per **claim 9**, Sample is directed to the apparatus in accordance with claim 8 wherein the network/resource interface circuit generates edges of the at least one clock signal in response to packets received via the network [0104-0106].

As per **claim 10**, Sample is directed to the apparatus in accordance wherein claim 8 wherein the network/resource interface circuit receives a primary clock signal generated external to the apparatus and generates edges of the at least one clock signal in response to edges of the primary clock signal [0116, 0118].

As per **claim 12**, Sample is directed to the apparatus in accordance with claim 8 further comprising conductors mounted on the circuit board for conveying at least output signal of each PLD as a clock gating signal input to the network/resource interface circuit, wherein the network/resource interface circuit generates the at least one clock signal as a function of a clock gating signal received from at least one of the PLDs [0017].

As per **claim 13**, Sample is directed to the apparatus in accordance with claim 5 further comprising: a plurality of cable connectors, each corresponding to a separate one of the PLDs, and signal paths coupling each cable connector to a second portion of the terminals of its corresponding PLD (figure 14; [0102]).

As per **claim 17**, Sample is directed to the apparatus in accordance with claim 6 wherein the network/resource interface circuit generates at least one clock signal, wherein the apparatus further comprises:

a. a local bus, formed on the circuit board and connected in parallel to a second subset of the terminals of each FPGA, for conveying input and output signals between each FPGA (figure 11 bus 4; figure 12 bus 202) and the network/resource interface circuit (figure 11 bus 310). The logic chip contains a VME interface (figure 20 interface 222) that is connected to the CPU (figure 20 processor 700) that provides the network interface. Thus 32 bit VME bus (figure 20 bus 600) allows exchange of data between the logic board and the CPU.

b. a clock bus mounted on the circuit board for concurrently delivering edges of the at least one clock signal to each FPGA for clocking logic circuits within the PLDs during the emulation [0104-0105].

c. conductors mounted on the circuit board for conveying at least output signal of each FPGA as a clock gating signal input to the network/resource interface circuit, wherein the network/resource interface circuits generates the at least one clock signal as a function of a clock gating signal received from at least one of the FPGAs [0017]. The conductors are connected to the input/output terminals of the programmable logic devices and thus are responsible for inputting and outputting signals to the board. Therefore, the clock signal [0014] coming out of the board is conveyed by the conductor.

As per **claim 19**, Sample is directed to the apparatus in accordance with claim 17 wherein the network/resource interface circuit generates edges of the at least one clock signal in response to packets received via the network [0086].

As per **claim 20**, Sample is directed to the apparatus in accordance wherein claim 17 wherein the network/resource interface circuit receives a primary clock signal generated external to the apparatus and generates edges of the at least one clock signal in response to edges of the primary clock signal [0086].

As per **claim 22**, Sample is directed to the apparatus in accordance with claim 17 further comprising: random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data conveyed by packets arriving via the network in the RAM prior to performing the emulation, and then controls states of inputs signals it transmits to the at least one emulation resource in response to the data it stored in the RAM [0111].

As per **claim 23**, Sample is directed to the apparatus in accordance with claim 17 further comprising: random access memory (RAM) mounted on the circuit board, wherein the network/resource interface circuit stores data representing states of output signals produced by the at least one emulation resource in the RAM during the emulation and thereafter transmits on the network packets conveying the data it stored in the RAM [0015], [0189], [0191].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample in view of Abramovici (US Patent No. 6,034,538).**

As per claim 4, Sample fails to disclose using the RAM to store configuration data.

Abramovici is directed to using reconfigurable hardware techniques to emulate hardware, and discloses using RAM to store configuration data for the FPGA (Abramovici: column 4 lines 8-15).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sample and Abramovici because the apparatus taught by Abramovici exploits run-time configuration in order to implement circuits much larger than the physical capacity of the reconfigurable hardware, while insulating the user from the underlying hardware and run-time infrastructure (Abramovici: column 2 lines 52-59).

3. **Claims 11 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample in view of Morris ('AnyBoard: An FPGA-based, Reconfigurable System').**

Sample discloses having the network interface circuit generate edges of the clock signal in response to edges of the primary clock signal (figures 19, 20; [0075], [0086]). The primary clock signal in the claim is analogous to the master clock signal disclose by Sample. The clock signal is generated on the

control board [0016-0017], which is connected to the logic board through the network interface circuit. Sample fails to disclose using an oscillator to generate a clock signal.

Morris is directed to a reconfigurable system that uses a plurality of FPGAs and RAMs to emulate a circuit design. Morris teaches the use of an oscillator to generate a clock signal (Morris: page 24).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sample and Morris because the architecture taught by Morris keeps costs low while providing the ability to handle a wide range of designs containing thousands to gates.

4. **Claims 14, 15, 16, 18, and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sample in view of Khalid ('Routing Architecture and Layout Syntheses for Multi-FPGA Systems' 1999).**

As per **claim 14**, Sample discloses connecting a FPGA to an external RAM and allows the communication of data between the two (figure 17 FPGA 304 RAM 302 bus 310). Sample also discloses connecting a plurality of FPGA chips to a single external SRAM [0101].

Sample does not disclose connecting a plurality of FPGAs to a plurality of RAMs

Khalid teaches a hardware prototyping system that uses three FPGAs for emulation, and connects each of the three FPGAs to its individual RAM (Khalid: figure 2-1; page 8, section 2.1.1).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sample and Khalid because the use of multiple RAMS with the plurality of FPGAs results in an inexpensive system that demonstrates the potential of multi-FPGA systems as an attractive and low-cost medium for rapid prototyping on many hardware designs (Khalid page 8 section 2.1.1).

As per **claim 15**, Sample discloses a plurality of cable connectors, each corresponding to a separate of the PLDs and signal paths coupling each cable connector to a second portion of the terminals of its corresponding PLD (figure 14; [0102]). Sample also discloses using switches to couple the RAM to the logic device [0083].

Sample does not disclose connecting a plurality of FPGAs to a plurality of RAMs

Khalid teaches a hardware prototyping system that uses three FPGAs for emulation, and connects each of the three FPGAs to its individual RAM (Khalid: figure 2-1; page 8, section 2.1.1). Khalid also discloses the use of switches in the interconnect of FPGAs and in the connections between the logic boards and RAM (Khalid: pages 12, 17, and 19).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sample and Khalid because the use of multiple RAMS with the plurality of FPGAs results in an inexpensive system that demonstrates the potential of multi-FPGA systems as an attractive and low-cost medium for rapid prototyping on many hardware designs (Khalid page 8 section 2.1.1).

As per **claim 16**, the combination of Sample and Khalid as applied to claim 15 above teaches the apparatus in accordance with claim 15 wherein the network/resource interface circuit controls the plurality of switches in response to data conveyed in packets received via the network (Khalid: section 3.3).

As per **claim 18**, Sample discloses a plurality of cable connectors, each corresponding to a separate of the PLDs and signal paths coupling each cable connector to a second portion of the

terminals of its corresponding PLD (figure 14; [0102]). Sample also discloses using switches to couple the RAM to the logic device [0083].

Sample does not disclose connecting a plurality of FPGAs to a plurality of RAMs

Khalid teaches a hardware prototyping system that uses three FPGAs for emulation, and connects each of the three FPGAs to its individual RAM (Khalid: figure 2-1; page 8, section 2.1.1). Khalid also discloses the use of switches in the interconnect of FPGAs and in the connections between the logic boards and RAM (Khalid: pages 12, 17, and 19), and using the network interface to control the switches (Khalid: section 3.3).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Sample and Khalid because the use of multiple RAMS with the plurality of FPGAs results in an inexpensive system that demonstrates the potential of multi-FPGA systems as an attractive and low-cost medium for rapid prototyping on many hardware designs (Khalid page 8 section 2.1.1).

As per **claim 24**, the combination of Sample and Khalid as applied to claim 15 above teaches the apparatus in accordance with claim 15 further comprising: another switch (S9) for selectively interconnecting signal paths between the second portion of the terminals of at least two of the PLDs (Khalid: section 3.3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

KAMINI SHAH
SUPERVISORY PATENT EXAMINER